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## TECHNICAL REPORT ECOM-O209-2

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# GUNN EFFECT DEVICES

QUARTERLY REPORT NO. 2

By

J. BARRERA

SEPTEMBER 1968

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UNITED STATES ARMY ELECTRONICS COMMAND • FORT MONMOUTH, N.J.

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HEWLETT-PACKARD COMPANY  
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Palo Alto, California

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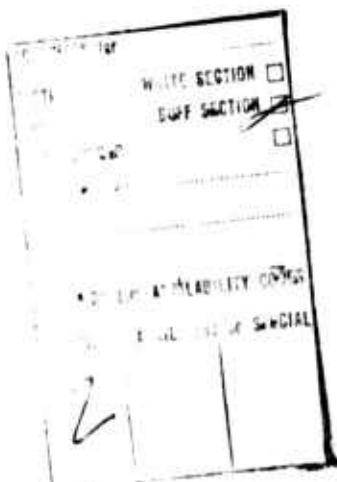
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GUNN EFFECT DEVICES

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15 March to 15 June 1968

October 1968

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Prepared by  
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HEWLETT-PACKARD COMPANY  
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U. S. Army Electronics Command, Fort Monmouth, New Jersey

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## SUMMARY

During the last quarterly period, time has been spent on organizing material requirements and setting up microwave and pulse bias circuitry along with producing initial runs of "scaled-up" CW units for use as pulse devices. Initial testing has shown efficiencies as high as 8% but more normally around 5 to 6 1/2%. Power levels were below 1 1/4 watts due to improper device fabrication but are expected to improve appreciably in future runs.

Thermal and geometrical considerations have been given to single and multiple unit sandwich type devices. Multiple chip unit problems were considered and various modes of operation have been studied for more efficient operation. LSA operating range has been considered to be too confined for low frequency operation in general. Hybrid mode and resonant transit time modes seem to hold more promise for achieving required pulse performance.

FOREWORD

The pulsed oscillator work reported in this quarterly report has been authorized by Contracting Officer S. M. Perkins, Procurement Division, United States Army Electronics Command, Fort Monmouth, New Jersey, under Contract No. DAAB07-68-C-0209.

The work has been performed under the supervision of Dr. M. M. Atalla. This report has been prepared by Dr. J. Barrera. Significant contributions have been made by Mr. T. Fortier, Mr. B. Farrell and Mrs. P. Clow. Discussions with Drs. G. W. Mathers and C. F. Quate have been of great benefit.

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## 1.

DEVICE PERFORMANCE

In accordance with the example pulse device design given in the last quarterly report, we have fabricated an initial run of devices labeled TE 298. The resistivity used was  $0.50 \Omega \text{ cm}$ , the length was  $16 \mu\text{m} \pm 1 \mu\text{m}$  and the dot contact was 12.7 mil diameter on a 25 mil chip. These dimensions are almost exactly as required by the design calculation given on pages 16 and 17 of the last quarterly report. After the final stage of preparation, the wafer was scribed and the 25 mil square samples separated. Unfortunately, the scribing and separating of these thin, yet large area chips resulted in partially cleaved areas on the chips, severe edge damage and tiny fractures. In addition, the electrical performance was quite obviously affected. The better looking chips were mounted on 75 mil diameter, gold plated, copper studs 300 mils long with a 10 mil high, 40 mil diameter pedestal under the chip. The low field resistance was from 0.90 to  $1.1 \Omega$  and the threshold voltage was from 5.2 to 5.9 volts. When pulsed, most of the units would not survive past 10 or 11 volts and were producing less than 400 mw peak power at 5% duty cycle for 1  $\mu\text{sec}$  pulse widths. The best appearing chips offered somewhat better performance and would withstand voltages approximately 3 times threshold voltage or about 16 to 18 volts. Typical 5% duty peak power was around 1 watt before the samples expired. Figure 1 shows device No. 6 peak power output as a function of voltage. The output frequency was varied from 5.3 to 5.7 GHz with much less than 0.5 db variation in power. The average efficiency was only 2.5%, which again points out the inherent inadequacy of this run of samples.

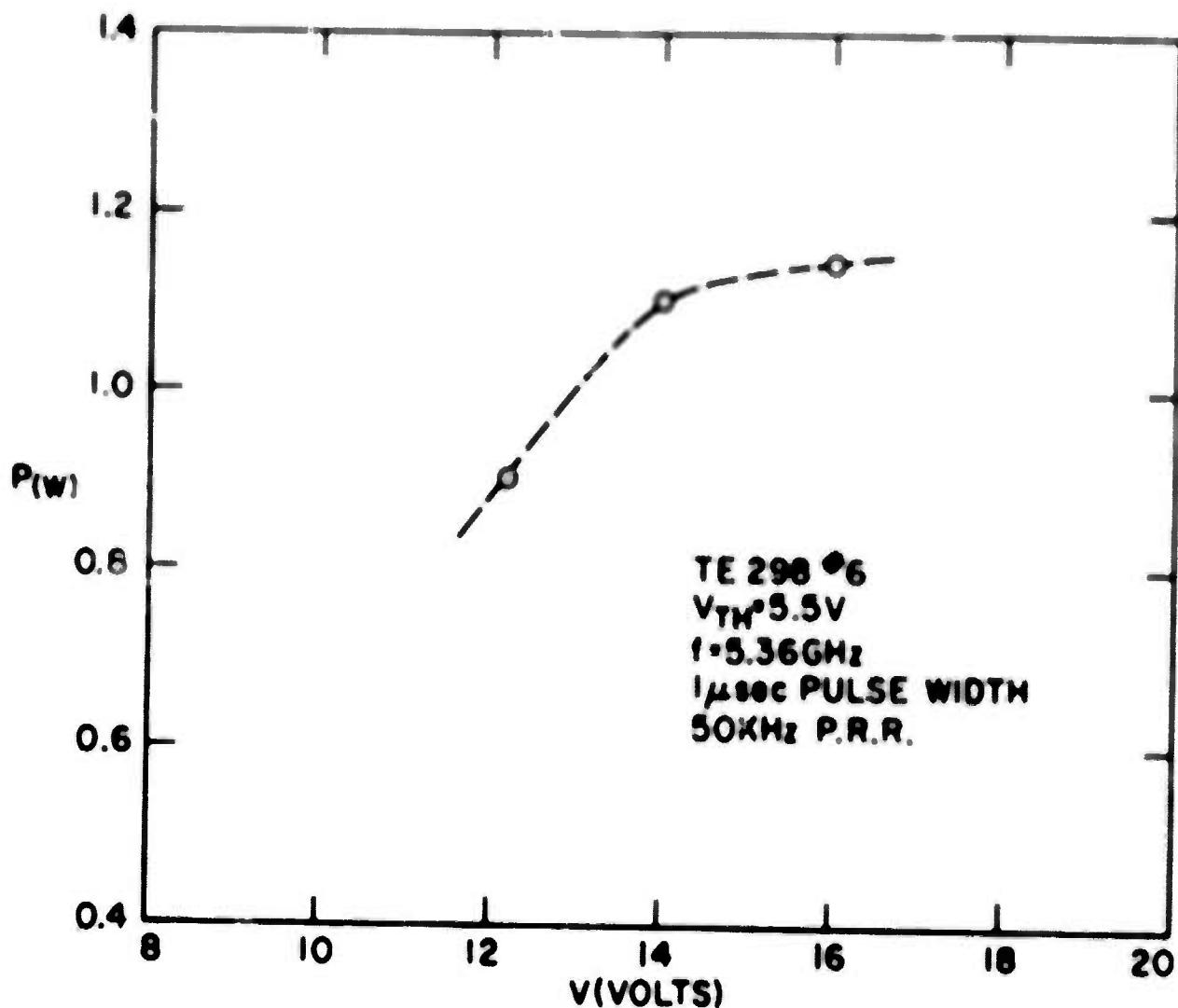


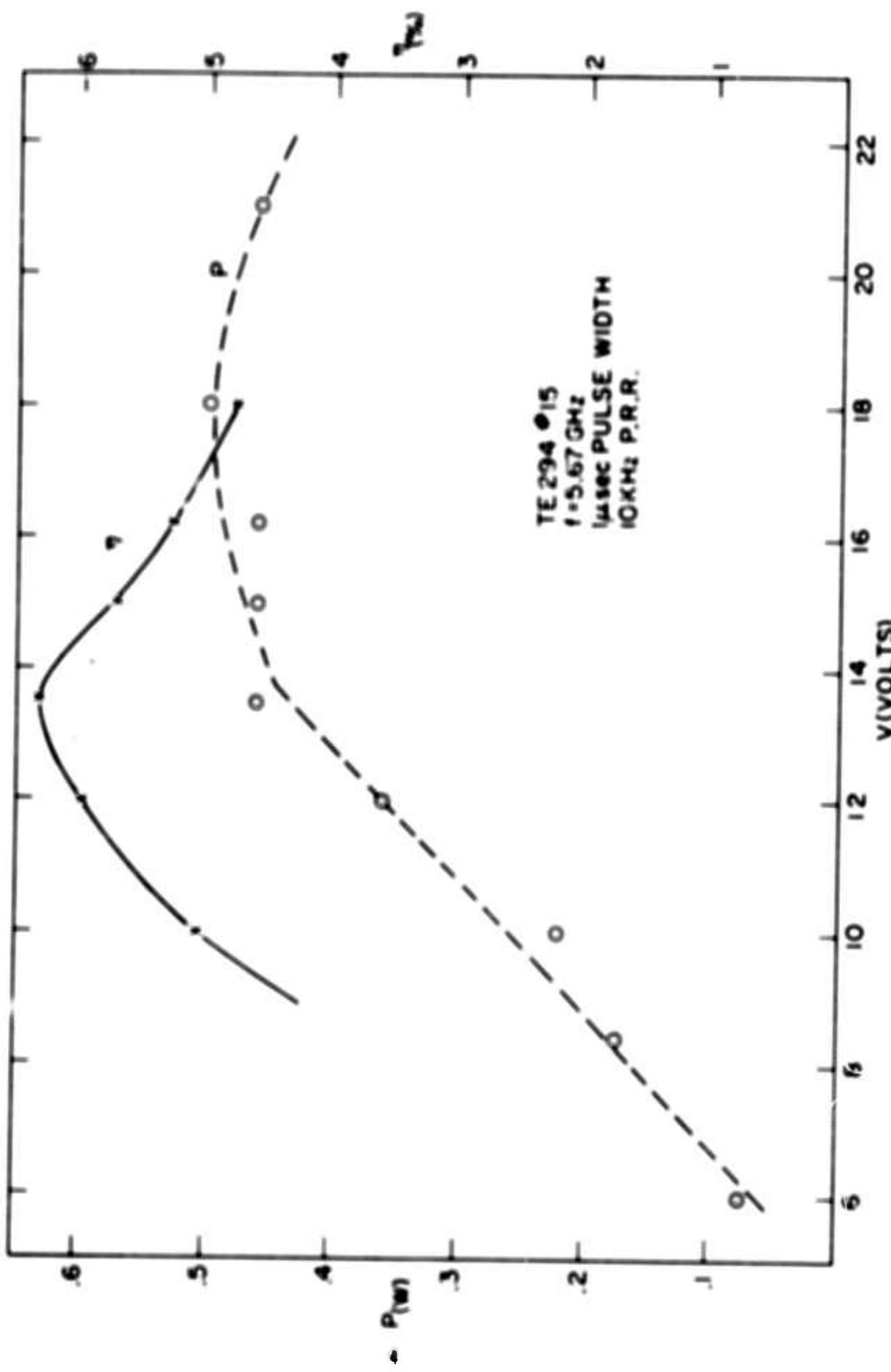
Figure 1. Peak Power vs. Bias.

It is felt that the biggest problem with the TI 290 devices was their inability to support sufficient bias voltage. Burning damage is the most probable cause since smaller area devices produced for CW operation and fabricated under identical conditions normally withstand pulse voltages of at least 10 to 11 times threshold (unbiased RF - wise). Fortunately, the problem is easily solved by etching samples out of the wafer. This will be done on the next run of scaled-up units.

As an interim measure and to further check the new microwave circuitry being used, it was decided to pulse some devices which were originally used for CW oscillators. Samples from runs TI 288, 291, 294, 316, and 320 were used. In general, their performance was quite good. In Figure 2 we show the 1% duty, peak power output, and efficiency which was typical of the above runs of devices. Peak powers of 1/2 watt were common with an occasional power reading of 900 mW being obtained. The efficiency was around 3 to 4.5% for bias voltages from 2.5 to 4.5 times threshold voltage. An efficiency as high as 7% could be achieved at 600 mW output for certain TI 292 devices. These devices were such that varactorities were from 0.50 to 0.780 cm, lengths were from 14 to 17 mm, and dot diameters were around 110  $\mu$ m. These figures reflect a power density of over 5  $\text{kW/cm}^2$ , consequently, the idea of scaling up the sample size to achieve the desired performance is still an encouraging one.

The biggest drawback, however, to the approach of building large devices (as intended with the TI 290 run) is impedance level. With low

Figure 2. Peak Power and Bit Error Rate vs. Bit rate



field resistances of 1 Ω or less, it becomes increasingly difficult to suppress bias circuit oscillations and to match or load the device properly. Also for the sub-Gunn frequency mode of operation, as presently being used, expected efficiencies are around 5 to 8%. This range of efficiency reflects back to expected peak power outputs of 5 watts or less when devices are designed as outlined in the last quarterly report. To obtain a desired output of 10 watts or more, we would have to parallel at least 2 or perhaps as many as 5 chips and accept the resultant low field resistance of 1/2 ohm or less. Although these drawbacks are significant, they are not so serious as to preclude investigation of the devices proposed.

There are other possibilities for using several scaled-up CW chips without suffering some of the above consequences. For example, it is perhaps possible to connect a few chips in parallel for D.C. operation, but have them connected in series RF-wise. This would improve the impedance problem significantly, but would certainly complicate the microwave circuitry. A push-push or properly phased push-pull operation would be mandatory.

The best solution would be, of course, to run devices in modes of operation where from 15 to 30% efficiency could be obtained. The resulting lower input power to achieve the derived output level would allow higher device impedances and would reduce the severity of the paralleling problems. Some of the possibilities will be discussed in a later section.

## II. MICROWAVE CIRCUITRY

The requirement of a fixed frequency of 5.675 GHz ( $\pm 10\%$  tuning bandwidth) makes the task of designing microwave cavities somewhat simpler than for wideband operation. Care must still be taken, however, since any higher order resonances might provide a better operating point for a sample at some particular bias voltages. For example, a coaxial resonator with a quarter wave resonance around 1 GHz will have  $3/4 \lambda$ ,  $5/4 \lambda$ ,  $7/4 \lambda$ , . . . resonances which are still within the operating range of a device that will perform well at 5 to 6 GHz. There are also possible ambiguities with waveguide cavities having the device mounted as part of a post in the guide. Here the basic resonance might be that of the post and device between the top and bottom wall shorts and conceivably might be below cut-off for the guide used. The detected radiation in this case would then only be lower power harmonics of the cut-off fundamental. In those waveguide cases where the detected radiation is indeed the fundamental and the cavity is formed between a sliding short and load, we find a significant amount of frequency pulling when the load is adjusted for maximum power output. It would be desirable then to build a cavity structure without high Q, higher resonance behavior, with only the desired output frequency, and with negligible frequency pulling upon loading.

We have had good success with a rather novel cavity structure that involves mounting the device in contact with a narrow gap, capacitive iris at the opening of a length of J-band (WH-127) guide. An X-band sliding

short is placed on the other side of the iris. Figure 3 shows a schematic of the total circuit used, and Figure 4 shows a photo of the iris flange itself. The sample is mounted on a stud as described in the previous section and the stud inserted in an anodized aluminum cylinder (also shown in Figure 4) which serves as the RF bypass capacitor. Figure 5 shows a photo of the iris flange and the J-band adapting flange mounted to an X-band sliding short. Note that the stud end and device are circled and that the particular iris shown has J-band height instead of X-band height as shown in Figure 4. The bias pulse is introduced through the top opening of the iris flange.

Looking across the guide, we see that the top of the iris and the top wall of the flange define a microstrip-like transmission line with some characteristic impedance  $Z_o$  terminated with shorts at either end. Figure 6 shows a sketch of the line defined and the placement of the sample. If the sample impedance is  $Z_C = \frac{-1}{Cw}$  and  $Z_L$  is the net reflected impedance at C, the resonance condition is met when  $|Z_L| = |Z_C|$ . The impedance  $Z_L$  is just the paralleled impedance  $Z_{L_1}$  given by

$$Z_{L_1} = jZ_o \tan \frac{2\pi}{\lambda} \frac{\ell}{2}$$

and thus

$$|Z_L| = \frac{Z_o}{2} \tan \frac{2\pi}{\lambda} \frac{\ell}{2} .$$

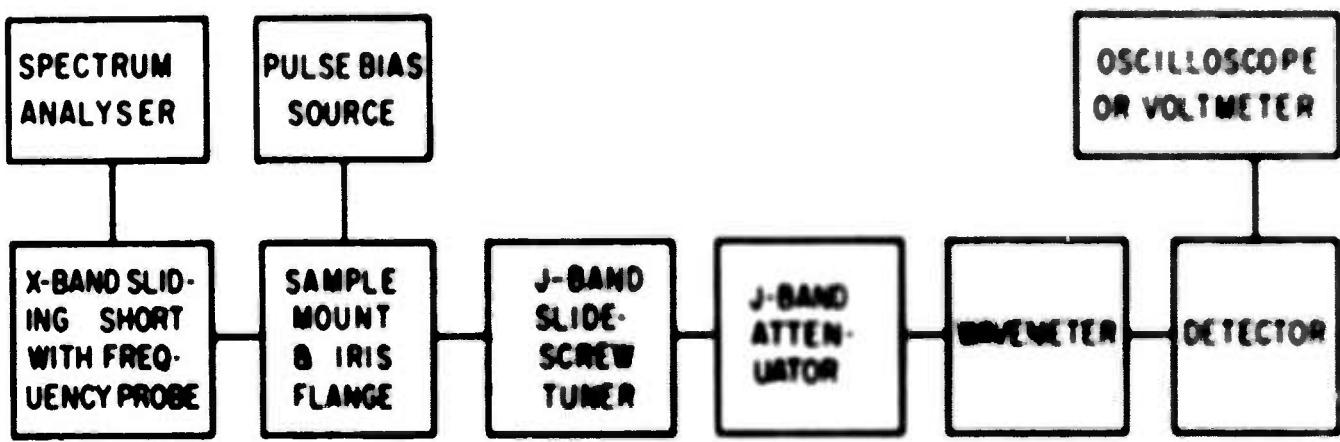
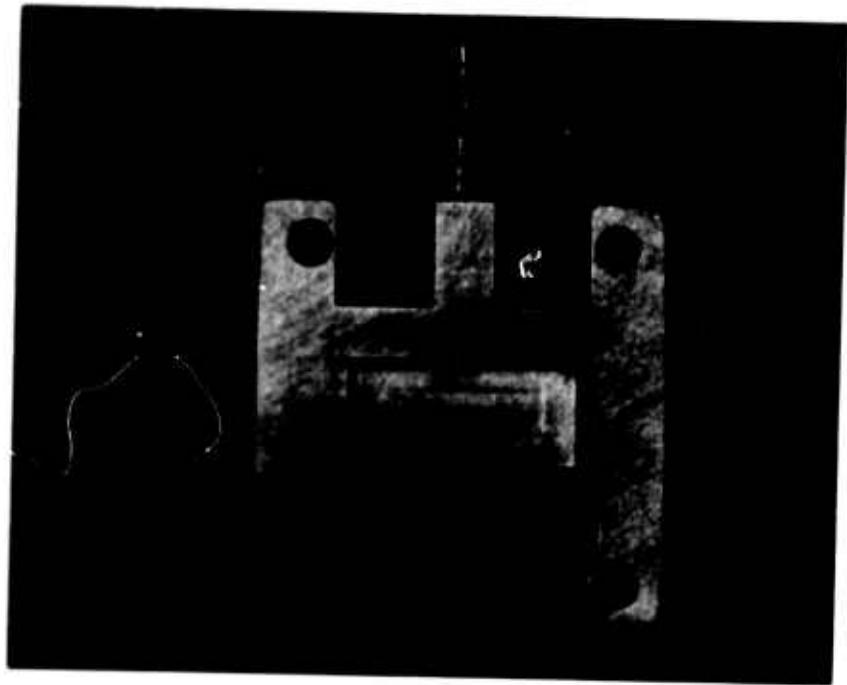
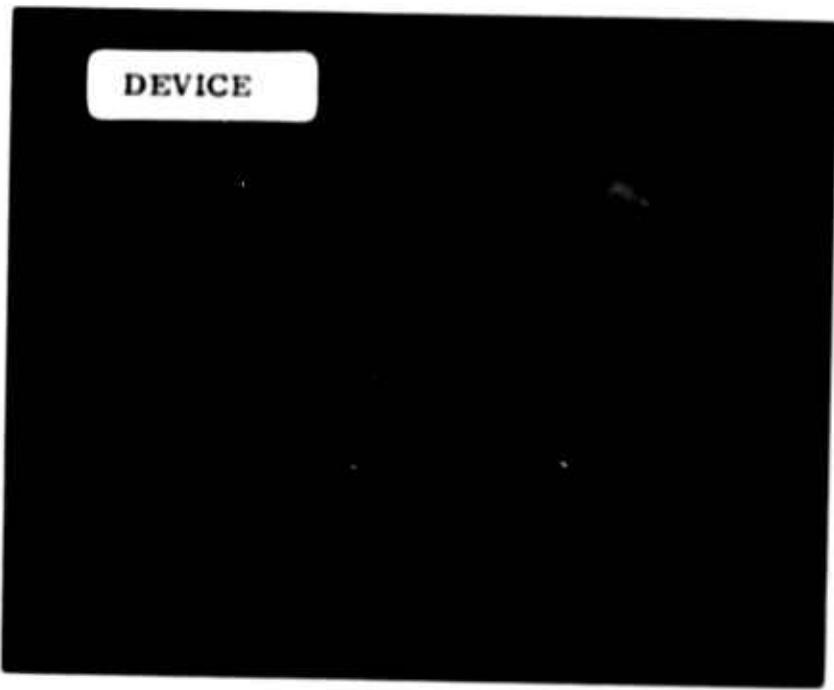


Figure 3. Circuit Schematic



**Figure 4. Iris Flange and Device Holder.**



**Figure 5. Mounted Iris Flange and J-Hard Adapter.**

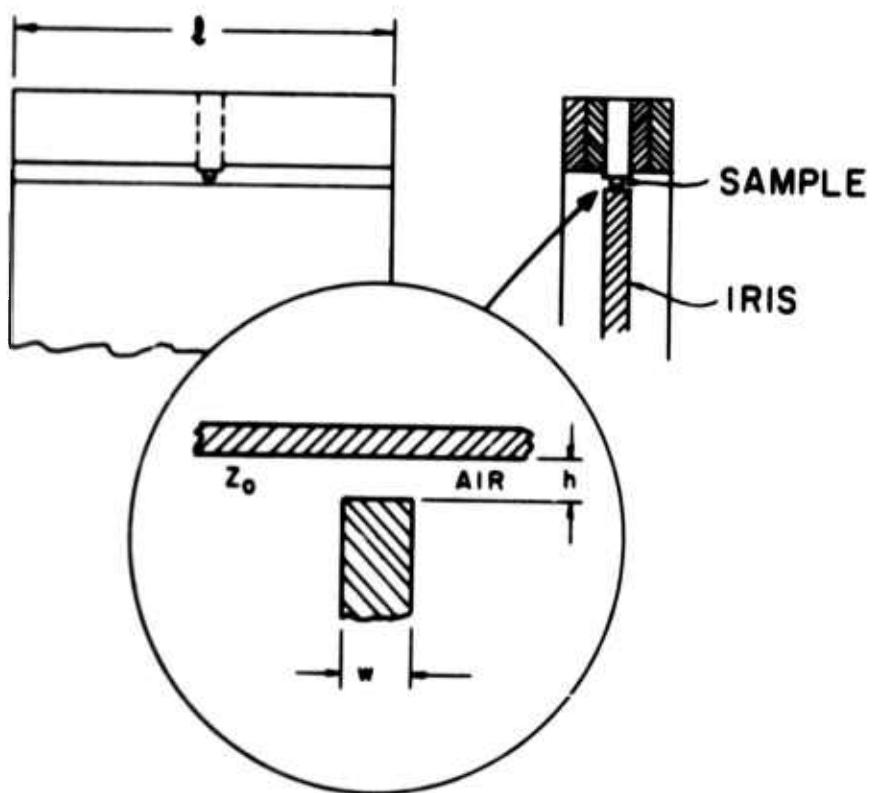


Figure 6. Iris Cross Section

At resonance

$$\frac{1}{C2\pi f} = \frac{Z_0}{2} \tan \frac{\pi l}{\lambda}$$

or finally,

$$f \tan \frac{\pi l}{v} = \frac{1}{\pi C Z_0}$$

where  $v$  is the wave velocity.

The above equation defines the cavity frequency when  $C$  and  $Z_0$  are known. Even without values for  $C$  and  $Z_0$ , we see that the unloaded resonance which supports a half wavelength equal to  $l$  is given by  $f = \frac{v}{2l}$ . For our case, X-band width is used which is cut off at 6.56 GHz ( $l = 0.900$  in). When loaded by the device impedance, the resonant frequency is accordingly lowered into the range desired. Final frequency trimming is accomplished by the X-band sliding short. Since the desired 5.675 GHz wave is very heavily attenuated, the short position affects the frequency only by very small amounts, which is all that is required. The device radiation is coupled out quite easily by the larger size guide on the other side of the iris and loading adjustment is provided by a slide screw tuner. Thus by adjusting the width  $l$  of the iris and the X-band short position, the desired 5.675 GHz resonance can be obtained for a fair range of sample capacitance. A further adjustment can be made by using iris flanges with different w/h ratios. This changes the effective  $Z_0$  of the

cross guide line and hence the resonant frequency. At present we are using a w/h ratio of 3.2 ( $h = 10$  mils), which for sample capacitances of about 0.5 pf gives a resonance around 5.5 GHz and a  $Z_0$  of  $\approx 20 \Omega$ . By changing the short position, tuning from 5 to 6 GHz can be achieved. In operation we have had no problem in setting the frequency where desired in the 5 to 6 GHz range, loading has been quite effective even for low resistance samples and frequency pulling at full load has not been a problem. With regard to higher order resonances, we see that the next frequency up would be a full wavelength over the length  $l$  or about 13.3 GHz unloaded. This mode is not possible, however, since it requires a nodal point at  $l/2$  where the device sits. Thus, the next resonance would be a  $3/4 \lambda$  mode or about 20 GHz unloaded, which for the samples to be considered is quite probably much above their operating range.

### III. MODES OF OPERATION

In section I we concluded with a rather obvious statement concerning the advantage of using high efficiency modes of operation. When one considers the prospect of obtaining high efficiency behavior from Gunn effect devices, very few real approaches come to mind. There have been many encouraging paper studies made of cavity controlled operation with results yielding "LSA," "quenched domain," "inhibited domain," "delayed domain," and, lately, "hybrid" mode categories, all with their respective recipes for the required parameter values for  $n_0$ , L, f, and  $V_{Bias}$ . In the world of numbers, one finds, however, that device performance most often has fallen quite short of expectations with efficiencies hovering around the 2 to 9% level as opposed to the hoped for 10 to 20% range. In those exceptional cases where efficiency has been quite high, the device physics has not really been understood or the operation has been at frequencies much lower than the 5 to 6 GHz range considered here.

There are many reasons why device performance is not as expected theoretically, but the basic point to be made is that there is not yet a clearcut practical approach to truly efficient device operation. Considering the case at hand, we can quite probably rule out trying the LSA mode of operation. Aside from what has been achieved experimentally by other workers (which is not very encouraging for efficient 5 to 6 GHz operation at high duty factors), we see that the LSA approach should be used in an inherently higher frequency range of operation where transit

time frequencies are much lower than operating frequencies, and hence samples are much longer than  $v_{peak}/f$ . Both experimentally and theoretically we find a prohibitively narrow range of parameters required to achieve LSA operation. The  $n_0/f$  and  $V_{Bias}$  range is indeed quite narrow around peak efficiency points, power output is a very sensitive function of loading, and RF field build-up time is quite critical in order to prevent domain formation and consequent field ionization destruction of samples.

The various other modes of operation can be classified as modified Gunn modes where cavity voltage is used to inhibit, quench, delay or initiate domains or partial domains and consequently deliver power to a load at the cavity frequency. The object for efficient operation is to have a load voltage waveform with a minimum of harmonic content and to accomplish a proper synchronization of cavity frequency with transit time frequency. In a recent paper by Carroll and Glibin<sup>1</sup>, most of the more important aspects of the possible modified domain modes are discussed and a good discussion given on the importance of proper synchronization of cavity voltage period with transit time.

In general, it appears that operation is best when output frequency is lower than the Gunn frequency although there is a resonant mode where operating frequency is twice the Gunn frequency, which allows good load voltage form and good efficiency but only under very specific operating conditions. There are other "resonant transit time" modes at one half and directly at the Gunn frequency which show very high efficiency but again are

difficult to realize practically because of the required precision of synchronization and operating conditions.

Recently, a so-called "hybrid" mode has been revealed<sup>2,3</sup> which is quite reasonably a mode of operation which covers the transition region between a true limited space charge condition to a space charge condition where one can no longer speak of fully formed transiting domains because of build-up times being on the order of an RF voltage period. Basically, one allows a dipole to form for a large portion of the RF period and then annihilates the resulting space charge distribution before it exits at the anode. The voltage swing must accordingly go below sustaining level and remain in the positive resistance region long enough to decay all space charge, thus insuring periodicity over one full RF voltage excursion. This mode of operation has been used with fairly good experimental success recently<sup>3</sup> with 15% efficiency having been realized at about 9 GigaHertz. There seems to be some discrepancy again between theoretical and experimental behavior with respect to the region of bias voltage and  $nl$  product allowed. However, in general the parameter value ranges seem to be rather broad and efficiencies should approach 20% in practice.

Considering the above discussion, it would seem that effort to achieve better efficiency from Gunn effect devices, as related to our problem, would best be placed on resonant transit time and hybrid type modes of operation. We will then consider the design, fabrication and testing of such devices during the following quarters along with a continuing effort on

the determination of the capabilities of scaled-up, 6% efficient devices as described earlier.

## IV.

 THERMAL AND GEOMETRICAL CONSIDERATIONS

Consideration must be given to thermal effects in this work because of the relatively high duty factors and required output power involved. For example, a 10% efficient device putting out 10 w peak power at 5% duty cycle will dissipate 5 watts average power. Depending on the thermal resistance of the sample and mount, a significant temperature rise can occur which may appreciably alter the peak to valley ratio and mobility of the GaAs material being used.

For a sandwich-type device, one can improve the thermal condition by "breaking" a large device into several smaller devices of equivalent total area. That is, on the assumption of an essentially constant power per unit area for a given mode of operation, we can deliver the same output power as from a large chip with several smaller chips and have the smaller chips running appreciably cooler than the single large chip. It has been shown in an earlier report<sup>4</sup> that the maximum steady state temperature rise in a sample of dot radius  $r$ , length  $l$  and die attach layer thickness  $d$  (see Figure 7) is given by

$$\Delta T = \frac{P_{in}}{\text{Vol.}} \cdot \left[ \frac{rl}{K_M} + \frac{l^2}{2K_S} + \frac{dl}{K_D} \right]$$

where the thermal conductivities are assumed temperature independent and heat sinking is on the die attach side only. From the above equation, we see that for a given power input per unit volume, the temperature rise is decreased as the dot radius and length are decreased. Consequently, by

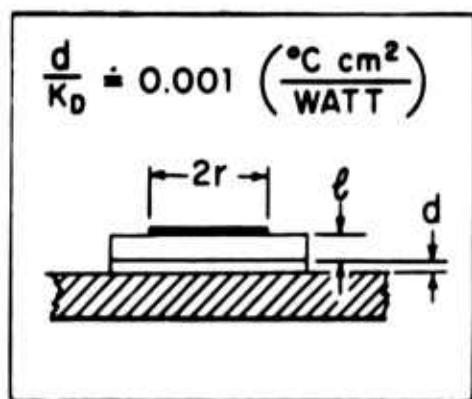


Figure 7. Geometrical Model for Thermal Calculation

dividing the 5 watts dissipated by the above example device into 1 watt amounts of dissipation from five smaller samples of total equivalent volume (or area since the length would be kept constant), we would expect an appreciable decrease in individual sample temperature rise.

For concreteness, let the large single chip be 16  $\mu\text{m}$  long and have a 205  $\mu\text{m}$  dot diameter. Its low field resistance would be 0.6  $\Omega$  for 0.5  $\Omega\text{cm}$  material, and it would deliver 10  $\times$  peak power at 5% duty cycle for 10% efficiency. The calculated thermal resistance for this sample would be  $\sim 6^\circ\text{C}/\text{watt}$  and for the 5 watts of dissipation we would have approximately  $30^\circ\text{C}$  temperature rise. Now, for five chips running in parallel and each having one-fifth the area, we find the dot diameter to be  $\sim 19^\circ\text{C}/\text{watt}$ . However, for the 1 watt dissipated by each chip we would have a temperature rise of only  $18^\circ\text{C}$ . Thus, a cooler running multiple-unit, equivalent to the single chip unit in resistance and output power would result.

Of course, this simple example assumes no disadvantage of running a multiple chip unit which, in practice, may not be true. Problems of mounting, contacting, operating coherently, and so forth might outweigh the advantages. However, the idea will be kept in mind for possible future use.

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